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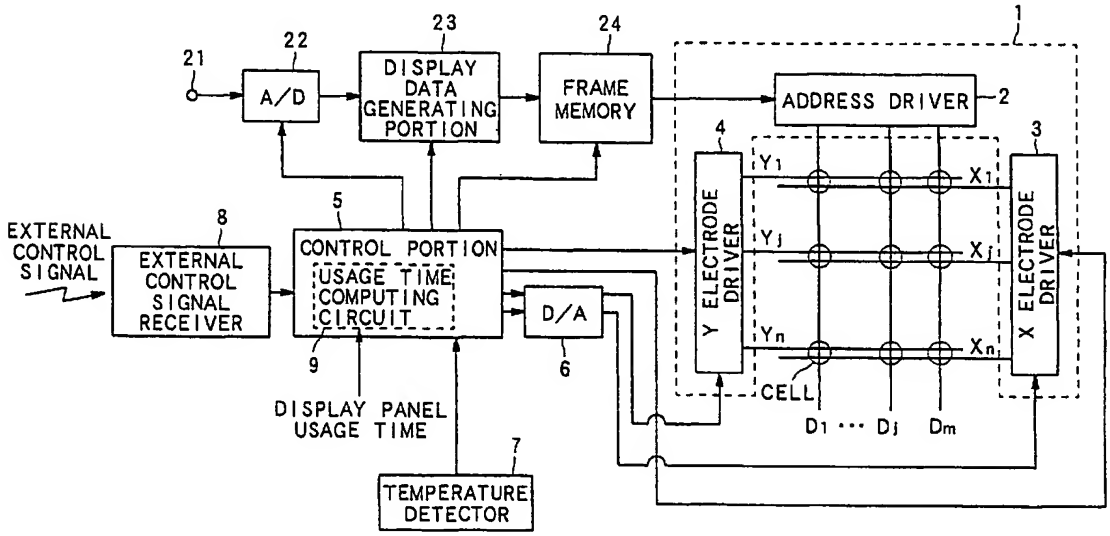
(54) Plasma display panel unit

(57) The plasma display panel (PDP) unit of the present invention comprises a PDP drive circuit (1) for supplying drive power to a display panel and a control portion (5) for controlling the drive power. The control portion (5) includes a power correction value generating circuit (5) for generating a power correction value and the PDP drive circuit (1) contains a voltage adjusting circuit (5) for outputting the drive power based on the power correction value.

FIG. 1



EP 1 271 464 A2

Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The present invention relates to technology relating to matrix type plasma display panel (PDP) and more particularly to technology relating to plasma display panel whose drive power supply is automatically adjusted.

2. Description of the Related Art

[0002] Conventionally, the drive voltage for a sustain driver and a scan driver has been adjusted by adjusting variable resistance upon shipment so as to secure an amount of margin corresponding to an influence upon the PDP by a change in temperature upon operation, a change of the PDP itself by time passage and the like. More specifically, a voltage adjusting circuit shown in FIG. 6 is inserted during a supply of electric power to the aforementioned driver and the variable resistor R63 is adjusted so as to correct the voltage of an input to an amplifier 60 thereby adjusting the driving voltage.

[0003] Conventional technology about the driving circuit of the PDP unit has been disclosed in Japanese Patent Application Laid-Open No. 2000-293135.

[0004] However, it takes skill for adjustment of this PDP and therefore there is a limit in reduction of adjustment cost. Further, there is a room in which human error may be induced.

[0005] The intensity of illumination is changed by a change in temperature at the time of startup and after long-hour use and this intensity of illumination is changed by a change with time passage of the PDP itself also. However, the change in the intensity of illumination in the PDP cannot be eliminated completely by adjustment of a single time before shipment.

[0006] In the above-mentioned Japanese Patent Application Laid-Open No. 2000-293135, the power supply is described only a symbol of the DC power supply in Fig.3, is not described about a voltage adjusting function.

SUMMARY OF THE INVENTION

[0007] An object of the present invention is to provide a PDP unit capable of eliminating human error upon adjustment of the PDP drive power and reducing cost.

[0008] The above object of the present invention can be achieved by a plasma display panel unit provided with: a panel driving device which supplies drive power to a display panel and a power control device which controls the drive power, wherein the power control device has a power correction value generating device which generates power correction value; and the panel driving device has a drive power changing device which changes and outputs the drive power based on the power correction value.

[0009] As a result, the drive power is changed based on the power correction value and outputted to the driver. Therefore, the drive power of the driver can be adjusted.

[0010] According to the present invention, automatic adjustment of the drive voltage is enabled. Thus, it is possible to omit voltage adjustment by skilled persons to eliminate human error completely and reduce cost.

[0011] The above object of the present invention can be achieved by a plasma display panel unit provided with a panel driving device which supplies drive power to a display panel and a voltage control device which control the voltage of the drive power, wherein the voltage control device has a voltage correction value generating device which generates voltage correction value; and the panel driving device has a drive voltage changing device which changes and outputs the drive voltage based on the voltage correction value.

[0012] Because the drive voltage is changed based on the voltage correction value and outputted to the driver, the drive voltage of the driver can be adjusted.

[0013] In one aspect of the plasma display panel unit of the present invention, the plasma display panel unit is further provided with at least any one of a temperature detecting device which detects the temperature of the display panel and a usage time computing device which computes usage time of the display panel, wherein the voltage correction value generating device generates the voltage correction value based on at least any one of a detected panel temperature and a measured usage time.

[0014] Because the control portion outputs the voltage correction value considering usage time or temperature of the panel, the drive voltage can be automatically adjusted corresponding to an influence by a change in the PDP temperature upon operation, changes in the PDP itself with time passage and the like.

[0015] Because the control portion can automatically output the voltage correction value and adjust the drive voltage considering panel usage time and panel temperature, it is possible to eliminate an influence by the temperature change in the PDP, an influence by the PDP itself with time passage and the like.

[0016] In another aspect of the plasma display panel unit of the present invention, the plasma display panel unit is further provided with an external control signal receiving device which receives an external control signal from outside, wherein the voltage correction value generating device generates the voltage correction value based on the external control signal.

[0017] Consequently, the control portion can receive the control signal from the remote controller, personal computer and the like and output the voltage correction value so as to adjust the drive voltage.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018]

FIG. 1 is a block diagram showing an outline of the PDP unit according to an embodiment of the present invention;

FIG. 2 is a schematic diagram showing the drive sequence of the PDP according to an embodiment of the present invention;

FIG. 3 is a conceptual diagram showing the structure of the PDP drive circuit according to an embodiment of the present invention;

FIG. 4 is an outline diagram of a voltage adjusting circuit according to an embodiment of the present invention;

FIG. 5 is a conceptual diagram showing the drive sequence of the PDP according to an embodiment of the present invention; and

FIG. 6 is a circuit diagram showing a conventional voltage adjusting circuit.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0019] Hereinafter, an embodiment of a plasma display panel (PDP) unit of the present invention will be described with reference to the accompanied drawings.

[0020] FIG. 1 is a block diagram showing an outline of the PDP unit.

[0021] The PDP unit comprises an input terminal 21, an A/D converter 22, a display data generating portion 23, a frame memory 24, a control portion 5, and a D/A converter 6. A PDP drive circuit acting as a panel driving device includes an address driver 2, an X electrode driver 3, and a Y electrode driver 4. Further, a PDP display unit includes a temperature detector 7 which works as a temperature detecting device for the display panel, a usage time counting circuit 9 which works as a usage time counting device for the display panel, and an external control signal receiver 8 which works as an external control signal receiving device.

[0022] A video signal inputted from the input terminal 21 is converted to digital video data by the A/D converter 22, processed to display data by the display data generating portion 23, and then supplied to the frame memory 24. The display data generating portion 23 computes emission time corresponding to the intensity of illumination of video data and corrects the data by reallocation so as to generate display data. The frame memory 24 is composed of, for example, a VRAM, which accumulates display data of a screen sent from the display data generating portion 23 and supplies it to the address driver 2 following synchronous signal from a control portion 5 which will be described later. The address driver 2 is composed of a driving circuit having a DC power supply and switching device, and generates pixel data pulse to each discharge cell on the display panel based on the display data inputted from a frame memory 24 and applies this to a column electrode Dj for every display line.

[0023] The control portion 5 is composed of, for example, CPU, which outputs synchronous signal to the A/D converter 22, the display data generating portion 23 and the frame memory 24. Further, the control portion 5, which works as a voltage control device, includes a voltage correction value generating circuit, which works as a voltage correction value generating device, so as to output a voltage correction value to adjust the PDP driving voltage. The D/A converter 6 converts the voltage correction value that the control portion 5 outputs in the form of digital value into an voltage correction value which is an analog signal and outputs it to an X-electrode driver 3 and a Y-electrode driver 4. As shown in FIG. 3, each of the X-electrode driver 3 and the Y-electrode driver 4 is constituted of a driving circuit containing a DC power supply and switching devices. Based on synchronous signal from the control portion 5, the X-electrode driver 3 applies sustain discharge pulse IPx to the electrode Xj and the Y-electrode driver 4 applies sustain discharge pulse IPy to the electrode Yj.

[0024] The temperature detector 7 of the display panel detects the temperature of a display panel and outputs the result of detection to the control portion 5. The usage time computing circuit 9 of the display panel computes a time in which the power of the display panel is turned ON and is part of the control portion 5. The external control signal receiver 8 receives a control signal from outside, for example, a remote controller or personal computer and outputs its content to the control portion 5.

[0025] The operation of the PDP unit having such a structure will be described below.

[0026] A video signal inputted from the input terminal 21 as an analog signal is converted to digital video data by the A/D converter 22, processed to display data by the display data generating portion 23, and supplied to the frame memory 24. The frame memory 24 accumulates display data sent from the display data generating portion 23 and supplies it to the address driver 2 following synchronous signal from the control portion 5.

[0027] A synchronous signal is separated from the video signal inputted from the input terminal 21 by a sync separation circuit (not shown), and then the control portion 5 outputs the synchronous signal to the A/D converter 22, the display data generating portion 23 and the frame memory 24 on the basis of this separated synchronous signal. The control portion 5 drives the PDP by controlling ON/OFF of a switching device of the PDP driving circuit 1, which is a panel driving device shown in FIG. 3. Additionally, the control portion 5 outputs an appropriate voltage correction value by computing a drive voltage of the PDP according to the result of temperature detection on the display panel and usage time of the display panel. Further, the control portion 5 receives a control signal from outside, for example, a remote controller or a personal computer, and computes

a voltage correction value depending upon its content, and outputs. At this time, the D/A converter 6 converts the voltage correction value to be outputted by the control portion 5 as digital value to analog value and outputs the result to the X electrode driver 3 or the Y electrode driver 4. Therefore, the control portion 5 facilitates adjustment of the driver voltage by means of a voltage adjusting circuit, which will be described later.

[0028] The drive sequence of the PDP unit will be described with reference to FIG. 2.

[0029] FIG. 2 is a schematic diagram showing the drive sequence of the PDP according to an embodiment of the present invention.

[0030] A set of a sub-field (1 SF) has a reset period, an address period, and a sustain period. A set of a field, which is a drive sequence of the PDP, has several subfields, repeated N times, and thereafter a main erase process for resetting to a condition in which wall charge is erased by applying erase pulse respectively to all cells.

[0031] In the reset period, all the discharge cells of the PDP unit are gotten into luminous discharge cell condition. In the subsequent address period, the address driver 2 forms wall charge selectively to each discharge cell based on video signal so as to generate pixel data pulse which sets up luminous discharge cell or non-luminous discharge cell and apply this pulse to a column electrode of every display line. In the sustain period, sustain discharge pulse IP_x and sustain discharge pulse IP_y are generated alternately and applied to the column electrode X and column electrode Y alternately. As a result, in a luminous discharge cell in which the above-described wall charge remains, discharge light emission is repeated and then that light emission is sustained.

[0032] The PDP unit of this embodiment adjusts the voltage of the X electrode driver 3 or the Y electrode driver 4 in the address period and the sustain period.

[0033] FIG. 3 is a conceptual diagram showing the structure of the PDP drive circuit 1 of this embodiment.

[0034] The PDP drive circuit 1, which works as a panel drive device, is comprised of the address driver 2, the X electrode driver 3, and the Y electrode driver 4. The X electrode driver 3 includes a reset pulse driver portion and a first sustain driver portion. The Y electrode driver 4 includes a reset pulse driver portion, a scan driver portion, and a second sustain driver portion.

[0035] The reset pulse driver portion applies a reset pulse respectively to all the column electrodes X_1-X_n, Y_1-Y_n at the same time in the reset period. Consequently, all the discharge cells in the PDP unit are simultaneously discharged and excited to generate charged particles. After this discharge is stopped, a predetermined quantity of wall charges are accumulated on a dielectric layer of the discharge cells, so that luminous discharge cell condition is attained.

[0036] The scan driver portion applies a scan pulse SP to the electrode Y_j in the address period so as to set the electrode Y_j to a predetermined positive potential (V_h - V_{off}). This application is carried out synchronously with application of pixel data pulse DP_j from the address driver 2. As a result, of the cells of the column electrode on which the scan pulse SP is applied, discharge occurs in only a cell onto which pixel data pulse of positive voltage is applied at the same time.

[0037] The first sustain driver portion and the second sustain driver portion generate sustain discharge pulse IP_x and sustain discharge pulse IP_y alternately in the sustain period and apply it to the column electrodes X_1-X_n and the column electrodes Y_1-Y_n alternately. Consequently, discharge light emission is repeated in the light emission discharge cell in which the wall charge remains, and the light emission is sustained.

[0038] The operation of the PDP drive circuit 1 having the above described structure will be described below.

[0039] The column electrode X_j is an electrode at the column j (one electrode composing the j display line) in the column electrodes X_1-X_n and the column electrode Y_j is an electrode at the column j (the other electrode composing the j display line) in the column electrodes Y_1-Y_n. The display panel cell is located between the column electrode X_j and Y_j which form a pair and acts as a capacitor C_o. A power supply B1 outputs sustain voltage V_{s1} and the voltage changes depending on an input of the voltage correction value from the control portion 5. A power supply B2 outputs a reset voltage V_{r1}.

[0040] The power supply B3 outputs the sustain voltage V_{s1} and the voltage changes depending on input of the voltage correction value from the control portion 5. The power supply B4 outputs the reset voltage V_{r1}. The power supply B5 generates the voltage V_{off} and the power supply B6 generates the scan pulse voltage V_h including the analog voltage correction value.

[0041] Because the voltage correction value can be inputted to the power supplies D1, B3, the sustain voltage can be adjusted and because the voltage correction value can be inputted to the power supply B6, the scan pulse voltage can be adjusted.

[0042] A voltage adjusting circuit for use in the sustain driver power supplies B1, B3 and the scan driver power supply B6 in the PDP drive circuit 1 having such a structure will be described below.

[0043] FIG. 4 is an outline diagram of the voltage adjusting circuit of this embodiment.

[0044] The voltage adjusting circuit of this embodiment is a drive voltage changing device and includes a loop circuit comprised of an amplifier, a transistor Tr and resistor R_{41} as shown in FIG. 4. Hereinafter, a loop gain is as A for describing.

[0045] Hereinafter, the operation of the voltage adjusting circuit having the above-described structure will be described.

[0046] If analog voltage $V_0 \pm \alpha$ containing $\pm \alpha$ analog voltage correction value in its original input voltage V_0 is inputted into the voltage adjusting circuit shown in FIG. 4 from the control portion, an increase/decrease amount $\Delta V_1 = \pm A \cdot \alpha$ is added to the original output volt-

age V_1 because the loop gain is A, so that the output voltage $V_1 \pm \Delta V_1$ is applied to the driver. Thus, the voltage correction value $\pm \Delta V_1$ acts on the driver so as to enable adjustment of the driver drive voltage.

[0047] The voltage adjusting circuit having such a structure is disposed at power supplies B1, B3, B6 of the PDP drive circuit 1 and the voltage correction value outputted from the control portion 5 is inputted as analog voltage correction value through the D/A converter 6. Thus, the sustain voltage can be adjusted at the power supplies B1 and B3. The scan pulse voltage can be adjusted at the power supply B6.

[0048] The operation of the PDP drive circuit 1 having such a structure will be described with reference to a time chart shown in FIG. 5. The drive sequence of this PDP describes the operation in a single sub-field. Subsequently, the reset period, address period, and sustain period will be described separately.

[0049] First, in the reset period, a switching device S8 of the X electrode driver 3 is turned ON, and at the same time, switching devices S16 and S22 of the Y electrode driver 4 are turned ON. The other switching devices are kept OFF. When the switching device S8 is turned ON, current flows from the electrode X_j to a negative terminal of the power supply B2 through a resistor R1 and a switching device S8. When the switching device S16 is turned ON, current flows into the electrode Y_j from a positive terminal of a power supply B4 through a switching device S16, a resistor R1, and a switching device S22. The potential of the electrode X_j is decreased gradually depending upon time constant of a capacitor C_o and the resistor R1 so that a reset pulse RP_x is generated. The potential of the electrode Y_j is increased gradually depending on time constant of the capacitor C_o and the resistor R1 so that a reset pulse RP_y is generated. Then, the potential of the reset pulse RP_x is saturated to the voltage level $-V_{r1}$, and the potential of the reset pulse RP_y is saturated to the voltage level V_{r1}. This reset pulse RP_x is applied to all the column electrodes X_1-X_n at the same time and the reset pulse RP_y is applied to all the column electrodes Y_1-Y_n simultaneously.

[0050] When these reset pulses RP_x, RP_y are applied at the same time, all discharge cells of the PDP are discharged and excited at the same time so as to generate charged particles. After this discharge is stopped, a predetermined quantity of wall charge is accumulated on dielectric layers of all discharge cells, so that luminous discharge cell condition is attained. When the reset pulses RP_x and RPy are saturated after a predetermined time interval elapses, the switching device S8 and the switching device S16 are turned OFF before the reset period is terminated. At the same time, the switching devices S4, S14 and S15 are turned ON and the electrodes X_j, Y_j are grounded. The reset period is terminated.

[0051] Next, in the address period, the address driver 2 forms wall charge selectively to each discharge cell based on display data outputted by the display data generating portion 23, pixel data pulses DP_1-DP_m generate and the pulses set the cells the luminous discharge cells or non-luminous discharge cells. This process is applied to the column electrodes D_1-D_m for every display line. Pixel data pulses DP_j, DP_{j+1} are applied to the electrodes Y_j, Y_{j+1}. When the address period is started, the switching devices S14 and S15 are turned OFF, and the switching devices S17 and S21 are turned ON, and simultaneously the switching device S22 is turned OFF. If the switching devices S17 and S21 are turned ON, positive potential (V_h-V_{off}) is applied to the electrode Y_j. Because as described above, the power supply B6 generates scan pulse voltage V_h containing analog voltage correction value, the positive potential (V_h-V_{off}), which is applied to the electrode Y_j at this time, also contains voltage correction value.

[0052] The switching device S21 is turned OFF synchronously with application of the pixel data pulse DP_j from the address driver 2 and then switching device S22 is turned ON. Consequently, a negative potential indicating the voltage $-V_{off}$ at a negative terminal of the power supply B5 is applied to as a scan pulse SP the electrode Y_j through the switching device S22. Then, the switching device S21 is turned ON synchronously with termination of the pixel data pulse DP_j from the address driver 2, and the switching device S22 is turned OFF, so that a predetermined positive potential (V_h-V_{off}) is applied to the electrode Y_j. After that, the scan pulse SP is applied to the electrode Y_{j+1} also synchronously with application of the pixel data pulse DP_{j+1} from the address driver 2 like the case of the electrode Y_j.

[0053] In the discharge cell belonging to the column electrode onto which the scan pulse SP is applied, discharge occurs only in a discharge cell onto which pixel data pulse of positive voltage is applied at the same time, so that wall charge of the cell erases. On the other hand, no discharge occurs in a discharge cell on which pixel data pulse of positive voltage is not applied at the same time although the scan pulse is applied and therefore, wall charge of the cell remains. In this case, the discharge cell in which the wall charge remains turns to a luminous discharge cell, while a discharge cell in which the wall charge is erased turns to a non-luminous discharge cell. When the address period is switched over to the sustain period, the switching devices S17 and S21 are turned OFF and at the same time, the switching devices S14, S15 and S22 are turned ON. The switching device S4 is kept ON.

[0054] Finally, the sustain period begins, the switching device S4 is turned OFF while the switching device S1 is turned ON. Consequently, current, whose origin is an electric charge accumulated in the capacitor C1, flows to the electrode X_j through a coil L1, a diode D1, and the switching device S1 to charge the capacitor C_o. At this time, the potential of the electrode X_j is raised gradually depending on time constant of the coil L1 and capacitor C_o. When half cycle of resonance cycle by the coil L1 and capacitor C_o elapses, the switching device S1 is turned OFF while the switching device S3 is turned

ON. Consequently, the potential of the electrode X_j turns to an equal potential to the sustain voltage V_{s1} containing the voltage correction value of the power supply B1.

[0055] After a predetermined time elapses, the switching device S3 is turned OFF while the switching device S2 is turned ON. As a result, current flows to the capacitor C1 through a coil L2, a diode D2 and the switching device S2 based on charge accumulated in the capacitor C_o so as to charge the capacitor C1. At this time, the potential of the electrode X_j lowers gradually depending on time constant of the coil L2 and capacitor C_o. When half cycle of resonance cycle by the coil L2 and capacitor C_o elapses (when the potential of the electrode X_j reaches 0V), the switching device S2 is turned OFF while the switching device S4 is turned ON.

[0056] By such operation, the X electrode driver 3 applies sustain discharge pulse IP_x to the electrode X_j. At the same time when the switching device S4 for erasing the sustain discharge pulse IP_x is turned ON, the Y electrode driver 4 turns ON the switching device S11 and turns OFF the switching device S14. When the switching device S14 is turned ON, the potential of the electrode Y_j is at grounding potential of 0V. When the switching device S11 is turned ON while the switching device S14 is turned OFF, current flows to the electrode Y_j through a coil L3, a diode D3, the switching device S11, a switching device S15 and a diode D6 based on electric charge accumulated on the capacitor C2 so that the capacitor C_o is charged. At this time, the potential at the electrode Y_j rises gradually depending upon time constant of the coil L3 and the capacitor C_o.

[0057] When the half cycle of resonance cycle by the coil L3 and the capacitor C_o elapses, the switching device S11 is turned OFF while the switching device S13 is turned ON. As a result, the potential of the electrode Y_j turns to an equal potential to the sustain voltage V_{s1} containing the voltage correction value of the power supply B3. If, after a predetermined time elapses, the switching device S13 is turned OFF while the switching device S12 is turned ON, current flows to the capacitor C2 through a switching device S22, a switching device S15, a coil L4, a diode D4 and the switching device 12 based on electric charge accumulated in the capacitor C_o so as to charge the capacitor C2.

[0058] At this time, the potential of the electrode Y_j drops gradually depending upon time constant of the coil L4 and capacitor C_o. When the half cycle of resonance cycle by the coil L4 and the capacitor C_o elapses (when the potential of the electrode Y_j reaches 0V), the switching device S12 is turned OFF while the switching device S14 is turned ON.

[0059] By such operation, the Y electrode driver 4 applies sustain discharge pulse IP_y of positive voltage to the electrode Y_j. In the sustain period, the sustain discharge pulse IP_x and the sustain discharge pulse IP_y are generated alternately and applied to the column electrode X_1-X_n and the column electrodes Y_1-Y_n alternately. As a result, the luminous discharge cell in which the wall charge remains repeats discharge light emission so as to sustain its light emission.

[0060] As shown in FIG. 1, the temperature detector 7 detects the temperature of the display panel, and the control portion 5 outputs a voltage correction value from that value. Because the drive voltage is adjusted through the D/A converter 6, automatic adjustment of the power voltage is enabled based on the panel temperature.

[0061] Further, because the control portion 5 is provided with the usage time computing circuit 9 for the display panel, it can output a voltage correction value corresponding to a passage time from the startup of the PDP unit, and can compute and output the voltage correction value by integrating PDP usage time and considering deterioration of brightness due to a change of the PDP with time passage. Because the analog voltage correction value is applied to the PDP drive circuit through the D/A converter 6, automatic adjustment of the drive voltage corresponding to the change of the PDP with time passage is enabled.

[0062] Further, by providing with the external control signal receiver 8 for receiving an external control signal from a remote controller, a personal computer or the like, the control portion 5 can output the voltage correction value corresponding to the external control signal so as to adjust the drive voltage. Consequently, the voltage can be adjusted by remote control or through the personal computer without removing a cover of the PDP main body.

[0063] The invention may be embodied in other specific forms without departing from the spirit or essential characteristics thereof. The present embodiments are therefore to be considered in all respects as illustrative and not restrictive, the scope of the invention being indicated by the appended claims rather than by the foregoing description and all changes which come within the meaning and range of equivalency of the claims are therefore intended to be embraced therein.

Claims

1. A plasma display panel (PDP) unit containing a panel driving device

   (1) which supplies drive power to a display panel and a power control device

   (5) which controls the drive power, **characterized in that**

   said power control device (5) has a power correction value generating device (5) which generates power correction value; and

   said panel driving device (1) has a drive power changing device (5) which changes and outputs the drive power based on said power correction value.

2. A plasma display panel (PDP) unit containing a panel driving device

(1) which supplies drive power to a display panel and a voltage control device
(5) which control the voltage of the drive power, **characterized in that**

said voltage control device (5) has a voltage correction value generating device (5) which generates voltage correction value; and

said panel driving device (1) has a drive voltage changing device (5) which changes and outputs the drive voltage based on said voltage correction value.

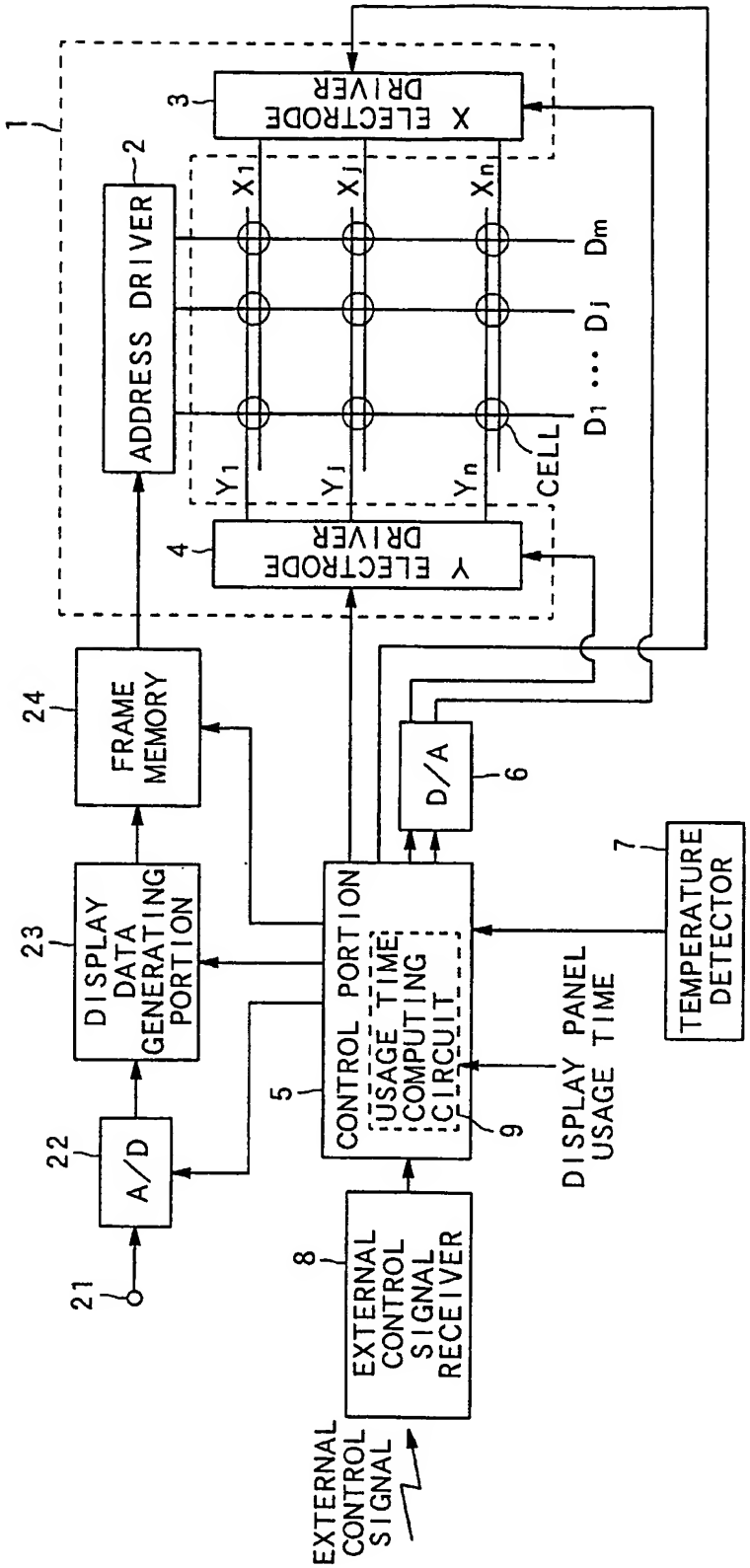
3. The plasma display panel (PDP) unit according to claim 2 containing at least any one of a temperature detecting device (7) which detects the temperature of the display panel and a usage time computing device (9) which computes usage time of the display panel, **characterized in that**

said voltage correction value generating device (5) generates the voltage correction value based on at least any one of a detected panel temperature and a measured usage time.

4. The plasma display panel (PDP) unit according to claim 2 further containing an external control signal receiving device (8) which receives an external control signal from outside, **characterized in that**

said voltage correction value generating device (5) generates the voltage correction value based on said external control signal.

FIG. 1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Xj
Xn
Y1
Yj
Yn
CELL
D1 ··· Dj Dm
21
22
A/D
23
DISPLAY DATA GENERATING PORTION
24
FRAME MEMORY
5
CONTROL PORTION
USAGE TIME COMPUTING CIRCUIT
9
6
D/A
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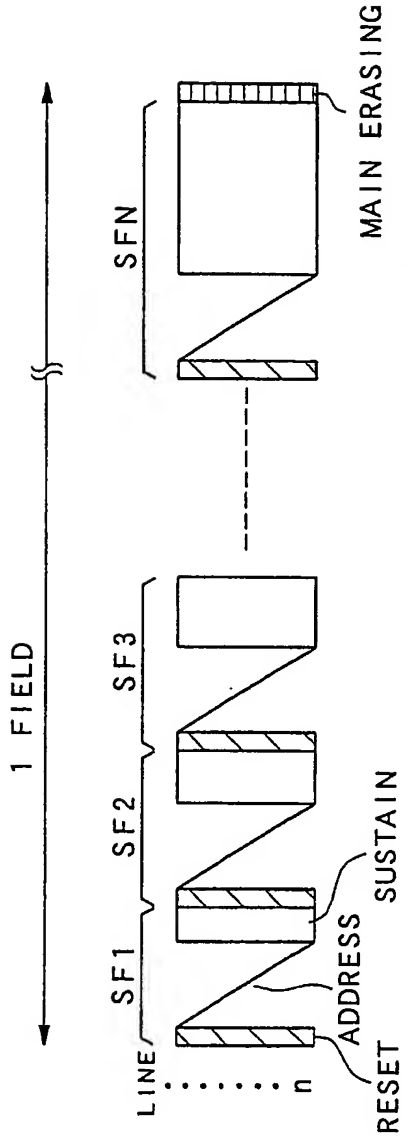
TEMPERATURE DETECTOR
8
EXTERNAL CONTROL SIGNAL RECEIVER
EXTERNAL CONTROL SIGNAL
DISPLAY PANEL USAGE TIME

FIG. 2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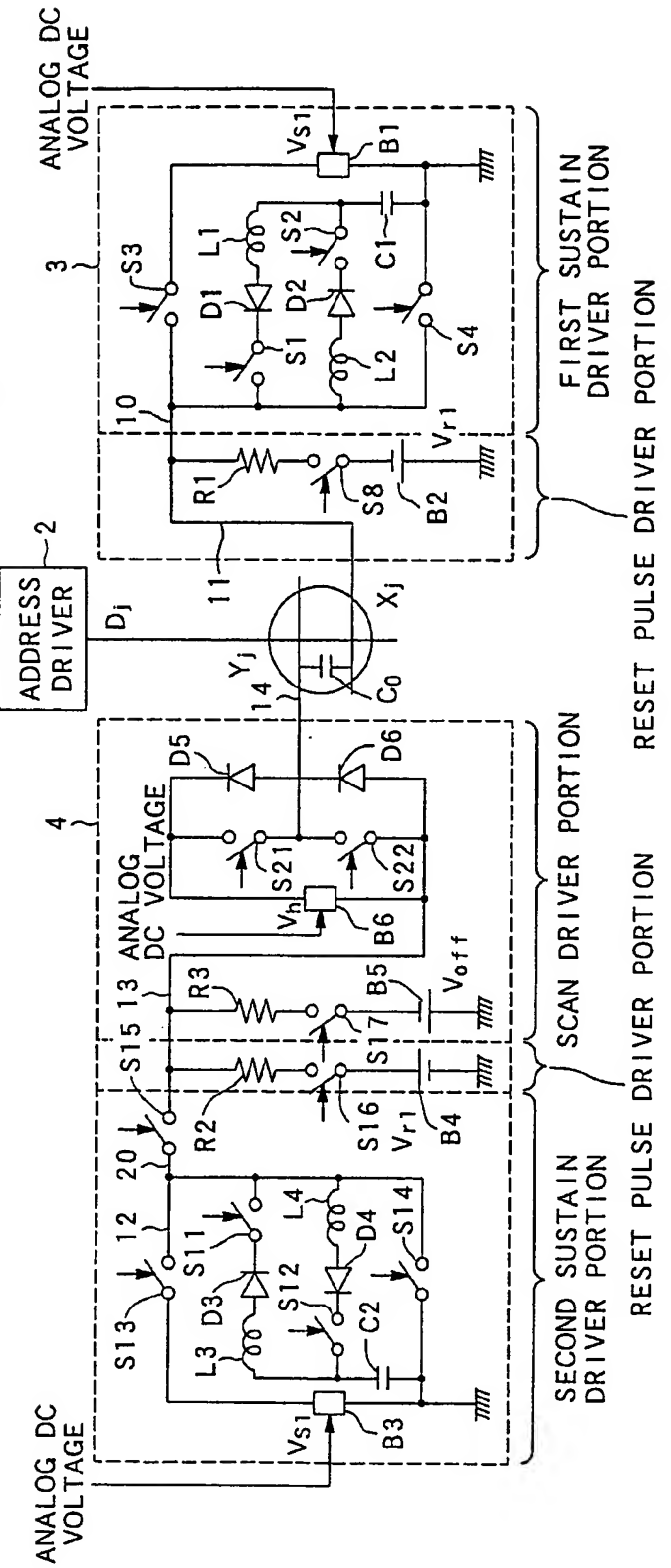
SF1
SF2
SF3
SFN
LINE
n
RESET
ADDRESS
SUSTAIN
MAIN ERASING

FIG. 3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2
ADDRESS DRIVER
3
4
ANALOG DC VOLTAGE
ANALOG DC VOLTAGE
ANALOG DC VOLTAGE
FIRST SUSTAIN DRIVER PORTION
RESET PULSE DRIVER PORTION
SCAN DRIVER PORTION
RESET PULSE DRIVER PORTION
SECOND SUSTAIN DRIVER PORTION
Dj
Xj
Yj
C0
L1
L2
L3
L4
D1
D2
D3
D4
D5
D6
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S2
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S4
S8
S11
S12
S13
S14
S15
S16
S17
S21
S22
C1
C2
R1
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R3
B1
B2
B3
B4
B5
B6
Vs1
Vr1
Vh
Voff
10
11
12
13
14
20

FIG. 4

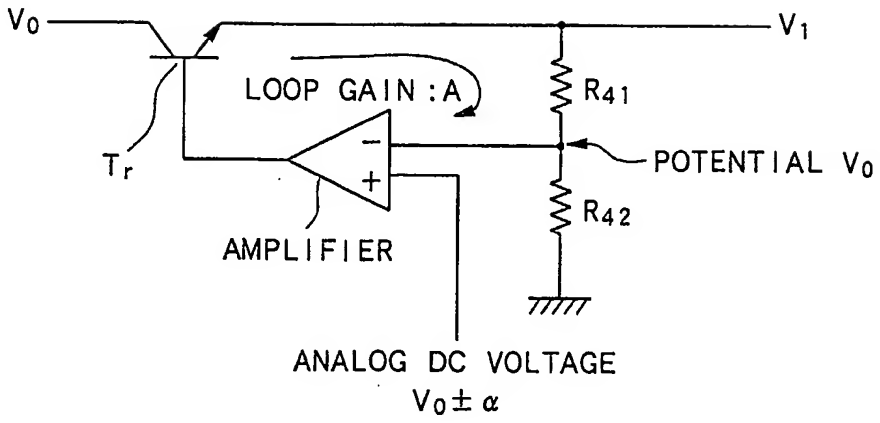
V0
V1
LOOP GAIN : A
R41
Tr
POTENTIAL V0
R42
AMPLIFIER
ANALOG DC VOLTAGE
V0 ± α

FIG. 5

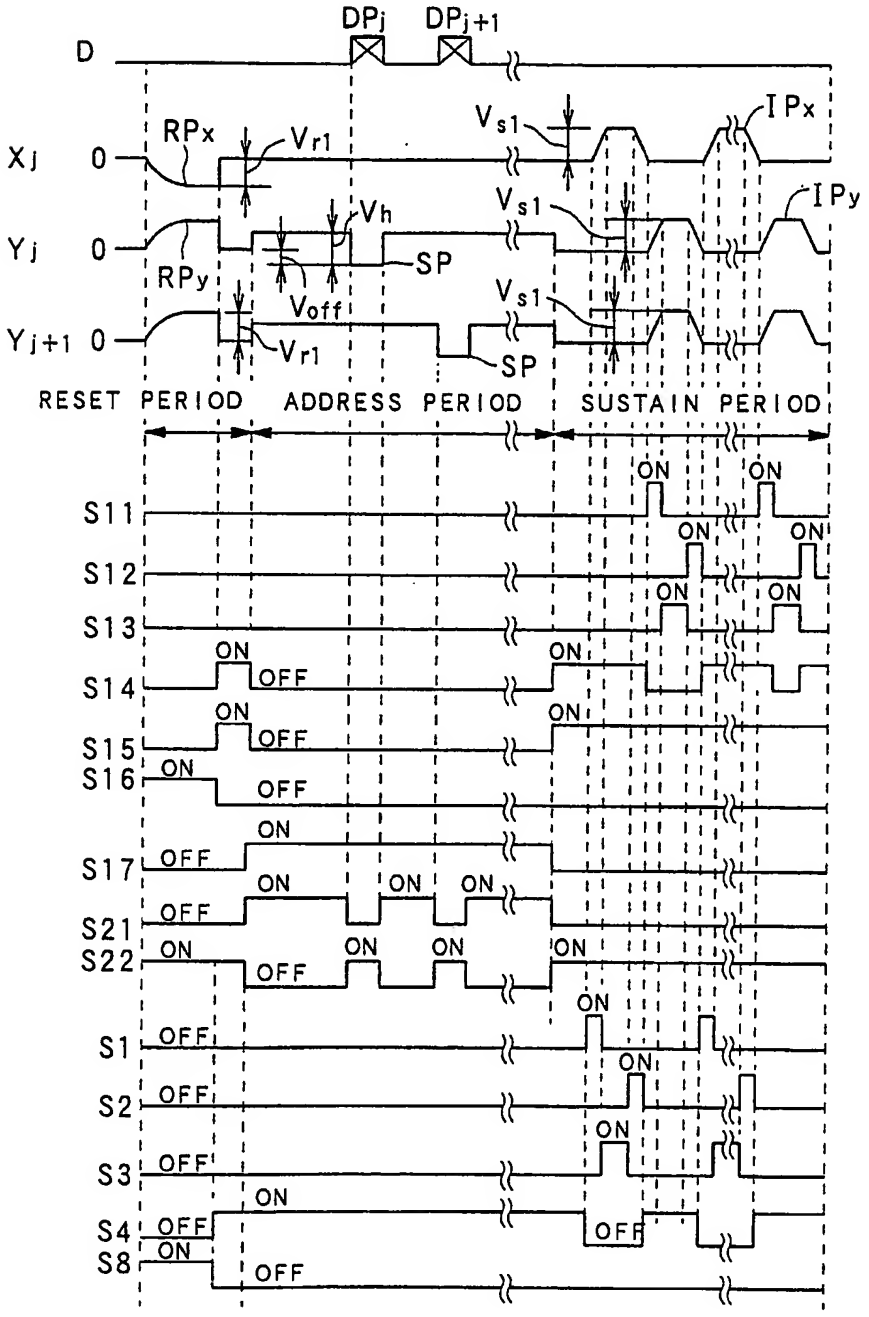
DPj
DPj+1
D
RPx
Vr1
Vs1
IPx
Xj
0
Vh
Vs1
IPy
Yj
0
RPy
SP
Voff
Vs1
Yj+1
0
Vr1
SP
RESET PERIOD
ADDRESS PERIOD
SUSTAIN PERIOD
S11
S12
S13
S14
S15
S16
S17
S21
S22
S1
S2
S3
S4
S8
ON
OFF

FIG. 6